

Device	Registers	Address	Int Vec-tor	Prior-ity	NPR
TA11	Cassette command & status data buffer	(TACS) 777 500 (TADB) 777 502	260	BR6	
TC11/ TU56	DECTape control & status command word count bus address data	(TCST) 777 340 (TCCM) 777 342 (TCWC) 777 344 (TCBA) 777 346 (TCDT) 777 350	214	BR6	X

**BM873-YA BOOTSTRAP LOADER:**

Starting Address	Device
773 000	RF11
773 010	RK11
773 020	Transfer to address contained in Switch Register
773 030	TC11
773 050	TM11
773 100	RP11
773 144	RC11
773 210	ASR paper tape reader
773 230	TA11
773 312	PC11

**BM873-YB BOOTSTRAP LOADER:**

Starting Address	Device
773 000	RJS03/RJS04 Disk Unit 0
773 002	RJS03/RJS04 Unit specified in console switch register
773 030	RK11 Disk Unit 0
773 032	RK11 Unit specified in console switch register
773 070	TC11
773 110	TM11
773 136	RF11
773 150	TJU16
773 212	RC11
773 320	RJP04 Disk Unit 0
773 322	RJP04 Unit specified in console switch register
773 344	Transfer to address in console switch register
773 350	RP11 Disk Unit 0
773 352	RP11 Unit specified in console switch register
773 510	KL11/DL11 Console TTY Reader
773 524	TA11 Cassette Unit 0
773 526	TA11 Unit specified in console switch register
773 620	PC11

**PDP-11/70 BOOTSTRAP LOADER:**

Starting Address 17 765 000

Device Type:	1	2	3	4	6	7	10	11	17	18
	TM11	TC11	RK11	RP11	TWU16	RWP04	RWS03/4	RX11		

**ABSOLUTE LOADER**

Starting Address: — 500  
Memory Size: —  
4K 017  
8K 037  
12K 057  
16K 077  
20K 117  
24K 137  
28K 157  
(or larger)

**BOOTSTRAP LOADER**

Address	Contents	Address	Contents
— 744	016 701	— 764	000 002
— 746	000 026	— 766	— 400
— 750	012 702	— 770	005 267
— 752	000 352	— 772	177 756
— 754	005 211	— 774	000 765
— 756	105 711	— 776	177 560 (TTY)
— 760	100 376		or 177 550(PC11)
— 762	116 162		

773 000 Paper Tape Bootstrap  
773 100 Disk/DECTape Bootstrap  
773 200 Card Reader Bootstrap  
773 300 Cassette Bootstrap  
773 400 Floppy Disk Bootstrap

**MR11-D8 BOOTSTRAP LOADER:**

Starting Address	Device
773 100	RF11
773 110	RK11
773 120	TC11
773 136	TM11
773 154	RP11
773 220	RC11

**7-BIT ASCII CODE:**

Octal Code	Char						
000	NUL	040	SP	100	@	140	\
001	SOH	041	!	101	A	141	a
002	STX	042	"	102	B	142	b
003	ETX	043	#	103	C	143	c
004	EOT	044	\$	104	D	144	d
005	ENQ	045	%	105	E	145	e
006	ACK	046	&	106	F	146	f
007	BEL	047	'	107	G	147	g
010	BS	050	(	110	H	150	h
011	HT	051	)	111	I	151	i
012	LF	052	*	112	J	152	j
013	VT	053	+	113	K	153	k
014	FF	054	,	114	L	154	l
015	CR	055	-	115	M	155	m
016	SO	056	.	116	N	156	n
017	SI	057	/	117	O	157	o
020	DLE	060	0	120	P	160	p
021	DC1	061	1	121	Q	161	q
022	DC2	062	2	122	R	162	r
023	DC3	063	3	123	S	163	s
024	DC4	064	4	124	T	164	t
025	NAK	065	5	125	U	165	u
026	SYN	066	6	126	V	166	v
027	ETB	067	7	127	W	167	w
030	CAN	070	8	130	X	170	x
031	EM	071	9	131	Y	171	y
032	SUB	072	:	132	Z	172	z
033	ESC	073	;	133	[	173	{
034	FS	074	<	134	\	174	
035	GS	075	=	135	]	175	}
036	RS	076	>	136	^	176	~
037	US	077	?	137	—	177	DEL



**PROGRAMMING CARD**

FOR FAMILY OF PDP-11 COMPUTERS

**WORD FORMAT:**



Mode	Name	Symbolic	Description
0	register	R	(R) is operand [ex. R2=%2]
1	register deferred	(R)	(R) is address
2	auto-increment	(R)+	(R) is adrs; (R) + (1 or 2)
3	auto-incr deferred	@(R)+	(R) is adrs of adrs; (R) + 2
4	auto-decrement	-(R)	(R) - (1 or 2); (R) is adrs
5	auto-decr deferred	@-(R)	(R) - 2; (R) is adrs of adrs
6	index	X(R)	(R) + X is adrs
7	index deferred	@X(R)	(R) + X is adrs of adrs

**PROGRAM COUNTER ADDRESSING:**

Reg = 7

Mode	Name	Symbolic	Description
2	immediate	#n	operand n follows instr
3	absolute	@#A	address A follows instr
6	relative	A	instr adrs + 4 + X is adrs
7	relative deferred	@A	instr adrs + 4 + X is adrs of adrs

**LEGEND:**

Op Codes	Operations
■ = 0 for word/1 for byte	( ) = contents of
SS = source field (6 bits)	s = contents of source
DD = destination field (6 bits)	d = contents of destination
R = gen register (3 bits), 0 to 7	r = contents of register
XXX = offset (8 bits), +127 to -128	← = becomes
N = number (3 bits)	X = relative address
NN = number (6 bits)	% = register definition

Boolean	Condition Codes
^ = AND	* = conditionally set/cleared
V = inclusive OR	- = not affected
∨ = exclusive OR	0 = cleared
~ = NOT	1 = set

**NOTE:**  
▲ = Applies to the 11/35, 11/40, 11/45 & 11/70 computers  
● = Applies to the 11/45 & 11/70 computers

**digital equipment corporation**

**DEVICE REGISTER ADDRESSES:**

Device	Registers	Address	Int Vec- tor	Prior- ity	NPR
CD11	Card Reader, high speed status & control column count current address data	(CDST) 777 160 (CDCC) 777 162 (CDBA) 777 164 (CDDB) 777 166	230	BR4	X
CR11	Card Reader status buffer, 12-bit char buffer, 8-bit char	(CRS) 777 160 (CRB1) 777 162 (CRB2) 777 164	230	BR6	
KW11-L	Line Clock	(LKS) 777 546	100	BR6	
KW11-P	Programmable Clock control & status count set buffer counter	772 540 772 542 772 544	104	BR6	
LA30, LA36, LT33, VT05, VT50	Console Terminal keyboard/reader status keyboard/reader buffer printer/punch status printer/punch buffer	777 560 777 562 777 564 777 566	60 64	BR4 BR4	
LP11, LS11, LV11	Line Printer printer status printer data	777 514 777 516	200	BR4	
PC11	Paper Tape reader status reader buffer punch status punch buffer	(PRS) 777 550 (PRB) 777 552 (PPS) 777 554 (PPB) 777 556	70 74	BR4 BR4	
RK11/ RK05	Disk Cartridge drive status error control & status word count current bus adrs disk address data buffer	(RKDS) 777 400 (RKER) 777 402 (RKCS) 777 404 (RKWC) 777 406 (RKBA) 777 410 (RKDA) 777 412 (RKDB) 777 416	220	BR5	X
RF11/ RS11	Disk disk control status word count current mem adrs disk address disk adrs ext & error disk data buffer maintenance adrs of disk segment	(DCS) 777 460 (WC) 777 462 (CMA) 777 464 (DAR) 777 466 (DAE) 777 470 (DBR) 777 472 (MA) 777 474 (ADS) 777 476	204	BR5	X
RP11-C/Disk RP03, RPR11/ RPR02	device status error control status word count bus address cylinder address disk address maintenance 1 maintenance 2 maintenance 3 selected unit cyl adrs silo memory	(RPDS) 776 710 (RPER) 776 712 (RPCS) 776 714 (RPWC) 776 716 (RPBA) 776 720 (RPCA) 776 722 (RPDA) 776 724 (RPM1) 776 726 (RPM2) 776 730 (RPM3) 776 732 (SUCA) 776 734 (SILO) 776 736	254	BR5	X
RX11/ RX01	Floppy Disk command & status data buffer	(RXCS) 777 170 (RXDB) 777 172	264	BR5	

Device	Registers	Address	Int Vec- tor	Prior- ity	NPR
RJP04/ RWP04/ RPO4	Disk control & status #1 word count UNIBUS address desired sector/track address RH11 control & status drive status error register #1 attention summary look ahead data buffer maintenance register drive type serial number offset desired cylinder current cylinder error #2 error #3 ECC position ECC pattern bus address ext control & status #3	(RPCS1) 776 700 (RPWC) 776 702 (RPBA) 776 704 (RPDA) 776 706 (RPCS2) 776 710 (RPDS) 776 712 (RPER1) 776 714 (RPAS) 776 716 (RPLA) 776 720 (RPDB) 776 722 (RPMR) 776 724 (RPDT) 776 726 (RPSN) 776 730 (RPOF) 776 732 (RPDC) 776 734 (RPCC) 776 736 (RPER2) 776 740 (RPER3) 776 740 (RPEC1) 776 744 (RPEC2) 776 746 (RPBAE) 776 750† (RPCS3) 776 752†	254*	BR5**	X
RJS04/ RWS04/ RS04, RJS03/ RWS03 RS03	Disk control & status #1 word count UNIBUS address desired disk adrs RH11 control & status drive status error attention summary look ahead data buffer maintenance drive type bus address ext control & status #3	(RSCS1) 772 040 (RSWC) 772 042 (RSBA) 772 044 (RSDA) 772 046 (RSCS2) 772 050 (RSDS) 772 052 (RSER) 772 054 (RSAS) 772 056 (RSLA) 772 060 (RSDB) 772 062 (RSMR) 772 064 (RSDT) 772 066 (RSBAE) 772 070† (RSCS3) 772 072†	204*	BR5**	X
TJU16/ TWU16/ TU16	Tape control & status #1 word count UNIBUS address frame count RH11 control & status drive status error attention summary check character data buffer maintenance drive type serial number tape control bus address ext control & status #3	(MTSC1) 772 440 (MTWC) 772 442 (MTBA) 772 444 (MTFC) 772 446 (MTCS2) 772 450 (MTDS) 772 452 (MTER) 772 454 (MTAS) 772 456 (MTCK) 772 460 (MTDB) 772 462 (MTMR) 772 464 (MTDT) 772 466 (MTSN) 772 470 (MTTC) 772 472 (MTBAE) 772 474† (MTCS3) 772 476†	224*	BR5**	X
TMA11/Magnetic Tape TU10, TS03	status command byte record cntr current mem adrs data buffer read lines	(MTS) 772 520 (MTC) 772 522 (MTBRC) 772 524 (MTCMA) 772 526 (MTD) 772 530 (MTRD) 772 532	224	BR5	X

\*Jumper Selectable

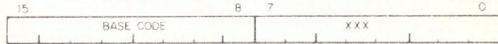
\*\*Plug Selectable

† Implemented on PDP-11/70 only

BRANCH: B -- location

If condition is satisfied:  
Branch to location,  
New PC ← Updated PC + (2 x offset)

adrs of br instr + 2



Op Code = Base Code + XXX

Mnemonic Base Code Instruction Branch Condition

**Branches**

BR	000400	branch (unconditional)	(always)
BNE	001000	br if not equal (to 0)	≠ 0 Z = 0
BEQ	001400	br if equal (to 0)	= 0 Z = 1
BPL	100000	branch if plus	+ N = 0
BMI	100400	branch if minus	- N = 1
BVC	102000	br if overflow is clear	V = 0
BVS	102400	br if overflow is set	V = 1
BCC	103000	br if carry is clear	C = 0
BCS	103400	br if carry is set	C = 1

**Signed Conditional Branches**

BGE	002000	br if greater or eq (to 0)	≥ 0 N+V = 0
BLT	002400	br if less than (0)	< 0 N+V = 1
BGT	003000	br if greater than (0)	> 0 Z v (N+V) = 0
BLE	003400	br if less or equal (to 0)	≤ 0 Z v (N+V) = 1

**Unsigned Conditional Branches**

BHI	101000	branch if higher	>> C v Z = 0
BLOS	101400	branch if lower or same	<< C v Z = 1
BHIS	103000	branch if higher or same	>= C = 0
BLO	103400	branch if lower	<= C = 1

**JUMP & SUBROUTINE:**

Mnemonic	Op Code	Instruction	Notes
JMP	0001DD	jump	PC ← dst
JSR	004RDD	jump to subroutine	} use same R
RTS	00020R	return from subroutine	
▲MARK	0064NN	mark	aid in subr return
▲SOB	077RNN	subtract 1 & br (if ≠ 0)	(R) - 1, then if (R) ≠ 0: PC ← Updated PC - (2 x NN)

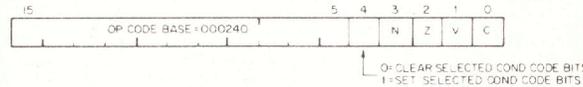
**TRAP & INTERRUPT:**

Mnemonic	Op Code	Instruction	Notes
EMT	104000 to 104377	emulator trap (not for general use)	PC at 30, PS at 32
TRAP	104400 to 104777	trap	PC at 34, PS at 36
BPT	000003	breakpoint trap	PC at 14, PS at 16
IOT	000004	input/output trap	PC at 20, PS at 22
RTI	000002	return from interrupt	
▲RTT	000006	return from interrupt	inhibit T bit trap

**MISCELLANEOUS:**

Mnemonic	Op Code	Instruction
HALT	000000	halt
WAIT	000001	wait for interrupt
RESET	000005	reset external bus
NOP	000240	(no operation)
●SPL	00023N	set priority level (to N)
▲MFP1	0065SS	move from previous instr space
▲MTP1	0066DD	move to previous instr space
●MFPD	1065SS	move from previous data space
●MTPD	1066DD	move to previous data space

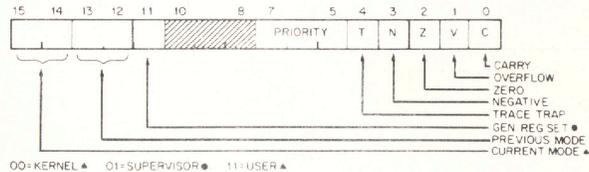
**CONDITION CODE OPERATORS:**



Mnemonic	Op Code	Instruction	N	Z	V	C
CLC	000241	clear C	-	-	-	0
CLV	000242	clear V	-	-	0	-
CLZ	000244	clear Z	-	0	-	-
CLN	000250	clear N	0	-	-	-
CCC	000257	clear all cc bits	0	0	0	0
SEC	000261	set C	-	-	-	1
SEV	000262	set V	-	-	1	-
SEZ	000264	set Z	-	1	-	-
SEN	000270	set N	1	-	-	-
SCC	000277	set all cc bits	1	1	1	1

**PROCESSOR REGISTER ADDRESSES:**

Processor Status Word  
PS - 777 776



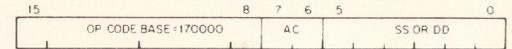
▲Stack Limit Register — 777 774

●Program Interrupt Request — 777 772

General Registers	R0 — 777 700	R4 — 777 704
(console use only)	R1 — 777 701	R5 — 777 705
	R2 — 777 702	R6 — 777 706
(not for 11/45)	R3 — 777 703	R7 — 777 707

Console Switches & Display Register — 777 570

**PDP-11/45, 11/70 FLOATING POINT PROCESSOR:**



Mnemonic	Op Code	Instruction	Operation
CFCC	170000	copy fl cond codes	FD ← 0
SETF	170001	set floating mode	FL ← 0
SETI	170002	set integer mode	FL ← 0
SETD	170011	set fl dbi mode	FD ← 1
SETL	170012	set long integer mode	FL ← 1
LDFPS	1701 src	load FPP prog status	
STFPS	1702 dst	store FPP prog status	
STST	1703 dst	store (exc codes & adrs)	
CLRf, CLRd	1704 fdst	clear floating/double	fdst ← 0
TSTf, TSTD	1705 fdst	test fl/dbl	
ABSF, ABSD	1706 fdst	make absolute fl/dbl	fdst ←  fdst
NEGF, NEGd	1707 fdst	negate fl/dbl	fdst ← -fdst
MULf, MULd	171 (AC) fsrc	multiply fl/dbl	AC ← AC x fsrc
MODf, MODd	171 (AC + 4) fsrc	multiply & integerize	
ADDf, ADDd	172 (AC) fsrc	add fl/dbl	AC ← AC + fsrc
LDF, LDD	172 (AC + 4) fsrc	load fl/dbl	AC ← fsrc
SUBf, SUBd	173 (AC) fsrc	subtract fl/dbl	AC ← AC - fsrc
CMFP, CMPD	173 (AC + 4) fsrc	compare fl/dbl (to AC)	
STf, STD	174 (AC) fdst	store fl/dbl	fdst ← AC
DIVf, DIVd	174 (AC + 4) fsrc	divide fl/dbl	AC ← AC/fsrc
STEXP	175 (AC) dst	store exponent	
STCFI, STCDFI	175 (AC + 4) dst	store & convert fl or dbi to int or long int	
STCDI, STCDL	175 (AC) fdst	store & convert (dbl-fl)	
STCDF, STCDFI	176 (AC) fdst	store & convert (dbl-fl)	
LDEXP	176 (AC + 4) src	load exponent	
LDCIF, LDCID	177 (AC) src	load & convert int or long int to fl or dbi	
LDCLF, LDCLL	177 (AC + 4) fsrc	load & convert (dbl-fl)	
LDCDF, LDCDFI	177 (AC + 4) fsrc	load & convert (dbl-fl)	

**PDP-11/35, 11/40 FLOATING POINT UNIT:**

Mnemonic	Op Code	Instruction	N	Z	V	C
FADD	07500R	floating add	*	*	0	0
FSUB	07501R	floating subtract	*	*	0	0
FMUL	07502R	floating multiply	*	*	0	0
FDIV	07503R	floating divide	*	*	0	0

**POWERS OF 2:**

n	2 <sup>n</sup>	n	2 <sup>n</sup>
0	1	10	1,024
1	2	11	2,048
2	4	12	4,096
3	8	13	8,192
4	16	14	16,384
5	32	15	32,768
6	64	16	65,536
7	128	17	131,072
8	256	18	262,144
9	512	19	524,288

PRINTED IN U.S.A. © 1975 DIGITAL EQUIPMENT CORPORATION



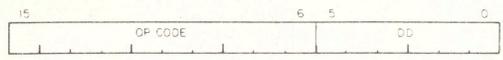
**NUMERICAL OP CODE LIST:**

OP Code	Mnemonic	OP Code	Mnemonic	OP Code	Mnemonic
00 00 00	HALT	00 60 DD	ROR	10 40 00	} EMT
00 00 01	WAIT	00 61 DD	ROL	↓	
00 00 02	RTI	00 62 DD	ASR	10 43 77	
00 00 03	BPT	00 63 DD	ASL	10 44 00	} TRAP
00 00 04	IOT	00 64 NN	MARK	↓	
00 00 05	RESET	00 65 SS	MFP1	10 47 77	
00 00 06	RTT	00 66 DD	MTP1		
00 00 07	(unused)	00 67 DD	SXT		
00 00 77	(unused)				
00 01 DD	JMP	00 70 00	(unused)	10 50 DD	CLRB
00 02 OR	RTS	00 77 77	(unused)	10 51 DD	COMB
00 02 10	(unused)	01 SS DD	MOV	10 52 DD	INCB
00 02 27	(unused)	02 SS DD	CMP	10 53 DD	DECB
00 02 3N	SPL	03 SS DD	BIT	10 54 DD	NEGB
00 02 40	NOP	04 SS DD	BIC	10 55 DD	ADCB
00 02 41	} cond codes	05 SS DD	BIS	10 56 DD	SBCB
00 02 77		06 SS DD	ADD	10 57 DD	TSTB
		07 0R SS	MUL	10 60 DD	RORB
00 03 DD	SWAB	07 1R SS	DIV	10 61 DD	ROLB
00 04 XXX	BR	07 2R SS	ASH	10 62 DD	ASRB
00 10 XXX	BNE	07 3R SS	ASHC	10 63 DD	ASLB
00 14 XXX	BEQ	07 4R DD	XOR	10 64 00	} (unused)
00 20 XXX	BGE	07 50 OR	FADD	10 64 77	
00 24 XXX	BLT	07 50 1R	FSUB	10 65 SS	MFPD
00 30 XXX	BGT	07 50 2R	FMUL	10 66 DD	MTPD
00 34 XXX	BLE	07 50 3R	FDIV	10 67 00	} (unused)
00 4R DD	JSR	07 67 77	(unused)	10 77 77	
00 50 DD	CLR	07 7R NN	SOB	11 SS DD	MOVB
00 51 DD	COM	10 00 XXX	BPL	12 SS DD	CMPB
00 52 DD	INC	10 04 XXX	BMI	13 SS DD	BITB
00 53 DD	DEC	10 10 XXX	BHI	14 SS DD	BICB
00 54 DD	NEG	10 14 XXX	BLOS	15 SS DD	BISB
00 55 DD	ADC	10 20 XXX	BVC	16 SS DD	SUB
00 56 DD	SBC	10 24 XXX	BVS	17 00 00	} floating point
00 57 DD	TST	10 30 XXX	BCC, BHIS	17 77 77	
		10 34 XXX	BCS, BLO		

**TRAP VECTORS:**

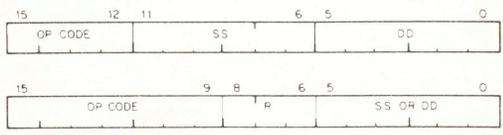
000	(reserved)	114	Memory Parity
004	Time Out & other errors	240	PIRQ, prog int req
010	illegal & reserved instr	244	Floating Point
014	BPT instruction	250	Memory Management
020	IOT instruction		
024	Power Fail		
030	EMT instruction		
034	TRAP instruction		

**SINGLE OPERAND: OPR dst**



Mnemonic	Op Code	Instruction	dst Result	N Z V C
<b>General</b>				
CLR(B)	050DD	clear	0	0 1 0 0
COM(B)	051DD	complement (1's)	$\sim d$	* * 0 1
INC(B)	052DD	increment	$d + 1$	* * * -
DEC(B)	053DD	decrement	$d - 1$	* * * -
NEG(B)	054DD	negate (2's compl)	$-d$	* * * -
TST(B)	057DD	test	$d$	* * 0 0
<b>Rotate &amp; Shift</b>				
ROR(B)	060DD	rotate right	$\rightarrow C, d$	* * * *
ROL(B)	061DD	rotate left	$C, d \leftarrow$	* * * *
ASR(B)	062DD	arith shift right	$d/2$	* * * *
ASL(B)	063DD	arith shift left	$2d$	* * * *
SWAB	0003DD	swap bytes		* * * 0
<b>Multiple Precision</b>				
ADC(B)	055DD	add carry	$d + C$	* * * *
SBC(B)	056DD	subtract carry	$d - C$	* * * *
▲SXT	0067DD	sign extend	0 or -1	- * 0 -

**DOUBLE OPERAND: OPR src, dst OPR src, R or OPR R, dst**



Mnemonic	Op Code	Instruction	Operation	N Z V C
<b>General</b>				
MOV(B)	1SSDD	move	$d \leftarrow s$	* * 0 -
CMP(B)	2SSDD	compare	$s - d$	* * * *
ADD	06SSDD	add	$d \leftarrow s + d$	* * * *
SUB	16SSDD	subtract	$d \leftarrow d - s$	* * * *
<b>Logical</b>				
BIT(B)	3SSDD	bit test (AND)	$s \wedge d$	* * 0 -
BIC(B)	4SSDD	bit clear	$d \leftarrow (\sim s) \wedge d$	* * 0 -
BIS(B)	5SSDD	bit set (OR)	$d \leftarrow s \vee d$	* * 0 -

**▲Register**

MUL	070RSS	multiply	$r \leftarrow r \times s$	* * 0 *
DIV	071RSS	divide	$r \leftarrow r/s$	* * * *
ASH	072RSS	shift arithmetically		* * * *
ASHC	073RSS	arith shift combined		* * * *
XOR	074RDD	exclusive OR	$d \leftarrow r \oplus d$	* * 0 -